Amendments to the Claims:

The following listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A method for fabricating a plurality of semiconductor bodies, comprising:

(a) forming a mask layer directly on a substrate comprising at least one material from the group consisting of silicon, silicon carbide and sapphire which mask layer has a plurality of windows leading to the substrate and onto which mask layer a semiconductor material, which is to be grown onto the substrate in a subsequent method step, substantially cannot be grown or can be grown to a significantly reduced extent by comparison with the substrate,

(b) etching back the substrate in the windows, in such a manner that pits are formed in the substrate starting from these windows,

(c) growing the semiconductor material onto the substrate, in such a manner that lateral growth is promoted and (i) the semiconductor material initially grows primarily from the flanks of the pits toward the center of the pits where the semiconductor material forms a coalescence region, so that defects in the substrate which impinge on the flanks of the pits bend off toward the center of the pits in the semiconductor material, and then (ii) the semiconductor material, starting from the windows, grows over the mask layer and in each case grows together over the mask layer

between adjacent windows, where the semiconductor material forms a further coalescence region, and

(d) growing a component layer sequence onto the semiconductor material.

2. (Previously presented) The method as claimed in claim 1, in which the growth of the semiconductor material is effected by means of metalorganic vapor phase epitaxy in an epitaxy reactor and mask material is applied to the substrate in the epitaxy reactor in such a manner that a discontinuous mask layer is formed, in which the windows leading to the substrate are already formed during the deposition of the mask layer.

3. (Canceled)

4. (Previously presented) The method as claimed in claim 1, in which a cross section of the pits perpendicular to the plane of the substrate is formed in a V shape or a U shape.

5. (Previously presented) The method as claimed in claim 1, in which the semiconductor material includes a plurality of layers of different compositions.

6. (Previously presented) The method as claimed in claim 1, in which the semiconductor material is grown using an ELOG technique.

7. (Previously presented) The method as claimed in claim 1, in which the semiconductor material which has grown has a substantially planar surface.

8. (Previously presented) The method as claimed in claim 1, in which the mask layer has a lattice-like or mesh-like structure.

9. (Previously presented) The method as claimed in claim 1, in which the mask layer contains silicon nitride.

10. (Currently amended) The method as claimed in claim 1, in which at least one element from the group consisting of the semiconductor material and the component layer sequence contains a compound of elements from the main groups III and V.

11. (Currently amended) The method as claimed in claim 1, in which at least one element from the group consisting of the semiconductor material and the component layer sequence contains a nitride compound semiconductor material.

12. (Previously presented) The method as claimed in claim 1, in which the semiconductor material contains a composition selected from the system $In_xAl_yGa_{1-x-y}N$, where $0 \leq x \leq 1$, $0 \leq y \leq 1$ and $x + y \leq 1$.

13. (Canceled)

14. (Currently amended) An electronic semiconductor body, comprising:

(a) a mask layer arranged directly on a substrate comprising at least one material from the group consisting of silicon, silicon carbide and sapphire, said mask layer having a plurality of windows leading to the substrate, and a semiconductor material arranged above the substrate, wherein said semiconductor material is constituted such that it substantially cannot be grown on the mask layer or can be grown on the mask layer to a significantly reduced extent in comparison with the substrate;

(b) pits in the substrate located within said windows, said pits being filled by the semiconductor material in such a manner that the semiconductor material has initially grown primarily from the flanks of the pits toward the center of the pits;

(c) at least one first coalescence region of the semiconductor material located in the pits, such that defects in the substrate which impinge on the flanks of the pits bend off toward the center of the pits in the semiconductor material;

(d) at least one second coalescence region located over the mask layer and between adjacent windows, said second coalescence region being surrounded by the semiconductor material; and

(e) a component layer sequence on the semiconductor material.

15. (Previously presented) The electronic semiconductor body as claimed in claim 14, which is a radiation-emitting semiconductor chip.

16. (Previously presented) The method as claimed in claim 1, wherein the plurality of semiconductor bodies comprise nitride compound semiconductor material.

17. (Previously presented) A method for fabricating a plurality of semiconductor bodies, comprising:

(a) forming a first mask layer over an underlying layer, wherein said first mask layer has a plurality of windows onto the underlying layer, and wherein said underlying layer comprises at least one of a substrate and an initial layer;

(b) etching, through the windows in the first mask layer, pits in the underlying layer; and

(c) depositing a first semiconductor material by:

(i) growing said first semiconductor material laterally from flanks of said pits in the underlying layer, wherein a first coalescence region is formed substantially in the center of each of said pits, wherein defects in the underlying layer which contact the sides of said pits propagate in said first semiconductor material in a lateral direction toward said first coalescence regions; and

(ii) growing said first semiconductor material outward from said windows, as said windows become full of deposited first semiconductor material, over said first mask layer, wherein second coalescence regions are formed above said first mask layer;

(d) forming a second mask layer on the first semiconductor material, said second mask layer having a plurality of windows onto the first semiconductor material; and

(e) through the windows of the second mask layer, depositing a second semiconductor material on said first semiconductor material.

18. (Previously presented) The method as claimed in claim 17, wherein the plurality of semiconductor bodies comprise nitride compound semiconductor material.

19. (Previously presented) The method as claimed in claim 17, further comprising forming a layer of said second semiconductor material above both said second mask layer and said first semiconductor material.

20. (Previously presented) The method as claimed in claim 19, further comprising forming a substantially planar surface on said layer of said second semiconductor material.

21. (Previously presented) The method as claimed in claim 20, further comprising growing a sequence of component layers on said substantially planar surface.